devices or device ranks that are targeted by relatively few logical-to-physical memory mappings, or by infrequent or non-recent memory accesses, and to set those devices or device ranks to a reduced power mode. Although in these examples the memory controller is responsible for identifying, tracking, and placing devices into a reduced power mode, it is possible for software (such as the operating system) to perform these functions as well.

Use Registers to Indicate In-Use Memory

In yet another embodiment, each memory device includes multiple dynamically changeable use registers such as described in a co-pending US patent application 09/919361 entitled "Monitoring In-Use Memory Areas for Power Conservation" by inventors Steven C. Woo and Pradeep Batra, filed concurrently herewith, which is hereby incorporated by reference.

Fig. 3 shows a memory device 40 that incorporates use registers 41 such as those referred to in the patent application mentioned above. These registers indicate used and unused memory cells or groups of used or unused memory cells. More specifically, use registers 41 in this embodiment comprise individual bits or flags that are associated respectively with individual memory cell rows 42. Each bit or flag is set to indicate whether or not the corresponding row is actually in use, and whether it therefore needs to be refreshed.

Memory controller 14 supports and maintains use registers 41 and allows them to be set or programmed by the operating system to indicate which memory rows are actually in use. For example, the operating system might set the use registers to indicate which rows of logical memory are currently allocated. As described in the previously mentioned patent application, use registers 41 allow